CLAIM AMENDMENTS

Please amend the claims by canceling claims 9 – 14, 16 and 31 – 37, amending claims 15, 17, 18, 19 and 21, and adding new claims 38 – 49, all without prejudice, as indicated on the following listing of all the claims in the present application after this Amendment:

1. – 8. (canceled)

9. – 14. (canceled)

15. (currently amended) A non-volatile memory cell array comprising a plurality of strings of series connected memory cells extending in a first direction across a semiconductor substrate, the memory cells including charge storage elements, the array including control lines extending in a second direction across the strings of memory cells and including control gates adjacent charge storage elements thereof, the first and second directions being orthogonal with each other, wherein the control gates are positioned between adjacent storage elements of the memory strings in a manner to be capacitively coupled with sidewalls of the adjacent storage elements of the memory cell strings on opposite sides of the control gates, wherein the control lines are additionally capacitively coupled with regions of the substrate between the storage elements in a manner to enhance the conductivity of the substrate regions in response to voltages placed on the control lines.

16. (cancelled)

17. (currently amended) ~~The~~ A memory cell array ~~of claim 16~~ comprising a plurality of strings of series connected memory cells extending in a first direction across a semiconductor substrate, the memory cells including charge storage elements, the array including control lines extending in a second direction across the strings of memory cells and including control gates adjacent charge storage elements thereof, the first and second directions being orthogonal with each other, wherein the control gates are positioned between adjacent storage elements of the memory strings in a manner to be capacitively coupled with sidewalls of the adjacent storage

elements of the memory cell strings on opposite sides of the control gates, wherein the control lines are additionally capacitively coupled with regions of the substrate between the storage elements and extend into trenches formed in the substrate regions with a layer of dielectric therebetween.

18. (currently amended) The memory cell array of ~~either of claims 11, 16 or~~ claim 17, wherein the capacitive coupling of the control lines with the substrate regions is characterized by enhancing the conductivity of the substrate regions in response to voltages placed on the control lines.

19. (currently amended) The memory cell array of claim ~~15~~ 17, wherein the charge storage elements include conductive floating gates that individually have heights extending above the substrate a distance that is larger than their widths, and wherein the control lines extend above the substrate at least as far as the heights of the floating gates to which the control gates are capacitively coupled.

20. (original) The memory cell array of claim 19, wherein a bottom portion of the control lines includes a doped polysilicon material and a top portion of the control lines includes a metal or silicide material in contact with the doped polysilicon material.

21. (currently amended) The memory cell array of ~~either one of claims 14 or~~ claim 20, wherein each of said control lines is positioned within the spacing between adjacent ones of the floating gates in order to be electrically isolated from one another.

22. (original) A non-volatile memory system, comprising:

a memory cell array, including:

a plurality of strings of series connected memory cells extending in a first direction across a semiconductor substrate and being spaced apart in a second direction, the first and second directions being perpendicular, the memory cells individually including a charge storage element, and

control gate lines extending in a second direction across multiple strings of memory cells and being positioned in the first direction between adjacent charge storage elements, wherein opposing sidewalls of individual charge storage elements are capacitively coupled with both of the control gates on opposite sides thereof, and

a voltage supply circuit connected to the control gate lines that simultaneously provides (a) first voltages to a pair of control gate lines on opposite sides of at least a first row of storage elements across the plurality of strings in order to raise voltage levels of at least the first row of storage elements to levels sufficient for altering or determining their charge states, and (b) a second voltage different from the first voltage to each of two control gate lines adjacent said pair of control gate lines on opposite sides thereof in the first direction in order to maintain voltage levels of charge storage elements in second and third rows on opposite sides of said at least the first row at levels insufficient for altering or determining their states.

23. (original) The memory system of claim 22, wherein the charge states number in excess of two, thereby enabling more than one bit of data to be stored in each memory cell.

24. (original) The memory system of claim 22, wherein the memory cell array is a NAND array.

25. (original) A method of making a memory cell array on a semiconductor substrate, comprising:

forming a rectangular array of columns and rows of floating gates across a surface area of the substrate with a first layer of dielectric therebetween,

providing isolation of the floating gates across the substrate between columns thereof, and

forming control gates extending across the substrate area perpendicular to said columns between rows of the floating gates in a manner that opposing sidewalls of the floating gates are capacitively coupled with walls of the control gates on opposite sides thereof through a second layer of dielectric and bottom surfaces of the control gates are capacitively coupled with the surface of the substrate over the well through a third layer of dielectric.

26. (original) The method of claim 25, wherein forming the floating gates includes:

depositing a layer of conductive floating gate material over the first layer of dielectric across the surface area of the substrate,

depositing a first type of dielectric material over the floating gate material layer,

removing portions of the first type of dielectric material to leave strips elongated in a direction of the columns and having widths and spaces between them in a direction of the rows according to a minimum resolvable element size,

forming spacers of a second type of dielectric along side walls of the strips of the first type of dielectric material in a manner leaving spaces between the spacers in the direction of the columns that are less than the minimum resolvable element size, and

removing portions of the first type of dielectric material and of the floating gate material layer between the spacers, thereby defining the floating gates with lengths and spaces between them in the direction of the columns that are less than the minimum resolvable element size.

27. (original) The method of claim 26, wherein removing portions of the first type of dielectric material includes forming a mask thereover with widths of strips and spaces therebetween according to the minimum resolvable element size, and thereafter isotropically sideways etching the first type of dielectric material through the mask in a manner that partially removes the first type of dielectric material under the mask strips, thereby to form the strips of the first type of dielectric material with widths that are less than the minimum resolvable element size.

28. (original) The method of either of claims 25 or 26, additionally comprising, prior to forming control gates, of forming trenches in the substrate surface between the floating gates in the direction of the columns, and wherein forming the control gates includes forming the control gates to extend into said trenches with electrical insulation therebetween.

29. (original) The method of either of claims 25 or 26, wherein forming the control gates includes forming a bottom portion of the control gates from doped polysilicon material and thereafter forming a top portion of the control gates from a metal or silicide material in contact with the doped polysilicon material.

30. (original) The method of claim 29, wherein forming the top portion of the control gates includes forming a continuous layer of said metal or silicide over the array, and thereafter performing a chemical-mechanical-polishing operation to remove an amount of said continuous layer that leaves the top portions of the control gates within the trenches and isolated from each other.

31. – 37. (cancelled)

38. (new) The memory cell array of claim 15, wherein the control lines extend into trenches formed in the substrate regions with a layer of dielectric therebetween.

39. (new) The memory cell array of claim 15, wherein the charge storage elements include conductive floating gates that individually have heights extending above the substrate a distance that is larger than their widths, and wherein the control lines extend above the substrate at least as far as the heights of the floating gates to which the control gates are capacitively coupled.

40. (new) The memory cell array of claim 39, wherein a bottom portion of the control lines includes a doped polysilicon material and a top portion of the control lines includes a metal or silicide material in contact with the doped polysilicon material.

41. (new) The memory cell array of claim 39, wherein each of said control lines is positioned within the spacing between adjacent ones of the floating gates in order to be electrically isolated from one another.

42. (new) The memory cell array of any one of claims 15, 17 – 21 and 38 – 41, wherein the control gates avoid overlapping tops of the adjacent storage elements and capacitive coupling therewith.

43. (new) The memory cell array of any one of claims 15, 17 – 21 and 38 – 41, wherein the storage elements are individually capacitively coupled with both of the control gates on opposite sides thereof.

44. (new) An array of non-volatile memory cells formed on a semiconductor substrate, comprising:

a plurality of strings of series connected memory cells extending in a first direction across the substrate and being spaced apart in a second direction, the first and second directions being perpendicular, the memory cells individually including a charge storage element, and

control gate lines extending in a second direction across multiple strings of memory cells and being positioned in the first direction between adjacent charge storage elements, wherein opposing sidewalls of individual charge storage elements are capacitively coupled with both of the control gates on opposite sides thereof.

45. (new) The memory cell array of claim 44, wherein the control gate lines extend into a trench formed in the substrate surface between the charge storage elements, with layers of dielectric positioned between the control gate lines and substrate surfaces of the trenches.

46. (new) The memory cell array of claim 44, wherein the control gate lines are capacitively coupled with regions of the substrate between the charge storage elements such that they enhance the conductivity of the substrate regions in response to voltages placed on the control gate lines.

47. (new) The memory cell array of claim 44, wherein the charge storage elements include conductive floating gates and the control gate lines extend above the substrate to at least a level of top surfaces of adjacent floating gates.

48. (new) The memory cell array of claim 47, wherein the control gate lines avoid overlapping the top surfaces of the adjacent storage elements and capacitive coupling therebetween.

49. (new) The memory cell array of any one of claims 44 – 46, wherein the strings of series connected memory cells individually include sixteen or more memory cells.